



# Exploration of Novel Tunnel Barrier Materials for STT-RAM

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Funded by DARPA and DMEA  
Collaborator: NIST, Freescale

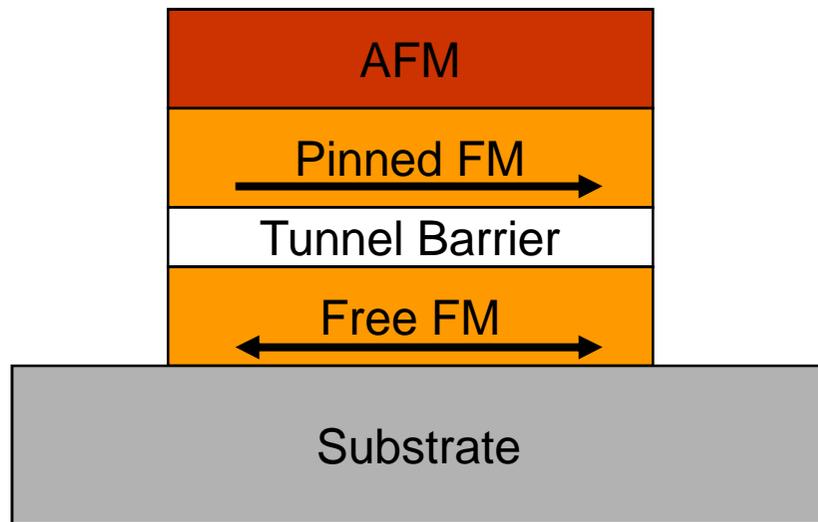
# Outline

- Introduction and Motivation
- Background Theory
- Experiment Setups
- Results & Discussion
- Summary & Future Plan

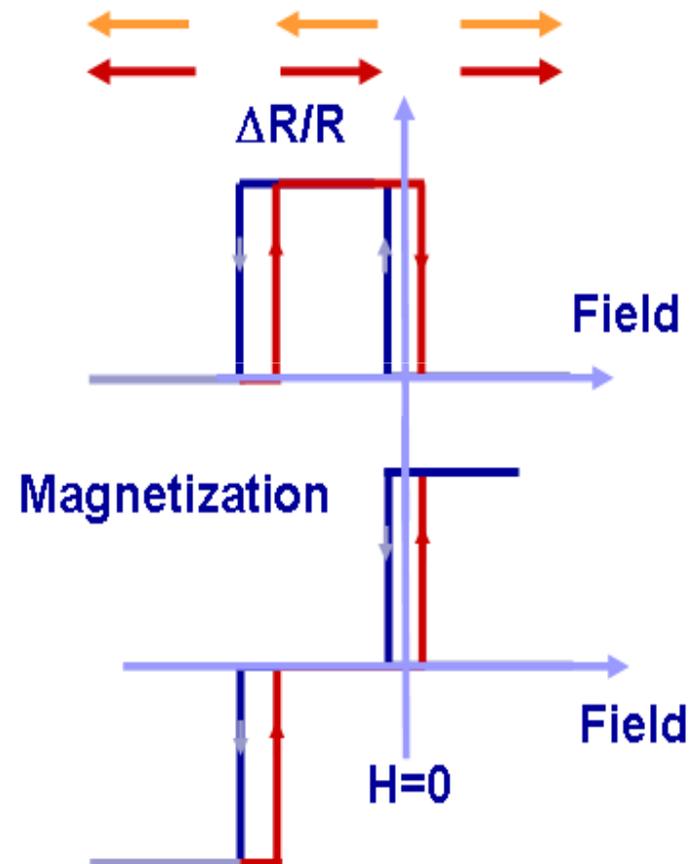
# Outline

- Introduction and Motivation
  - What is Magnetic Tunnel Junction (MTJ)?
  - MRAM: Major Application of MTJ
  - New Solution: Spin Torque Transfer!
- Background Theory
- Experiment Setups
- Results & Discussion
- Summary & Future Plan

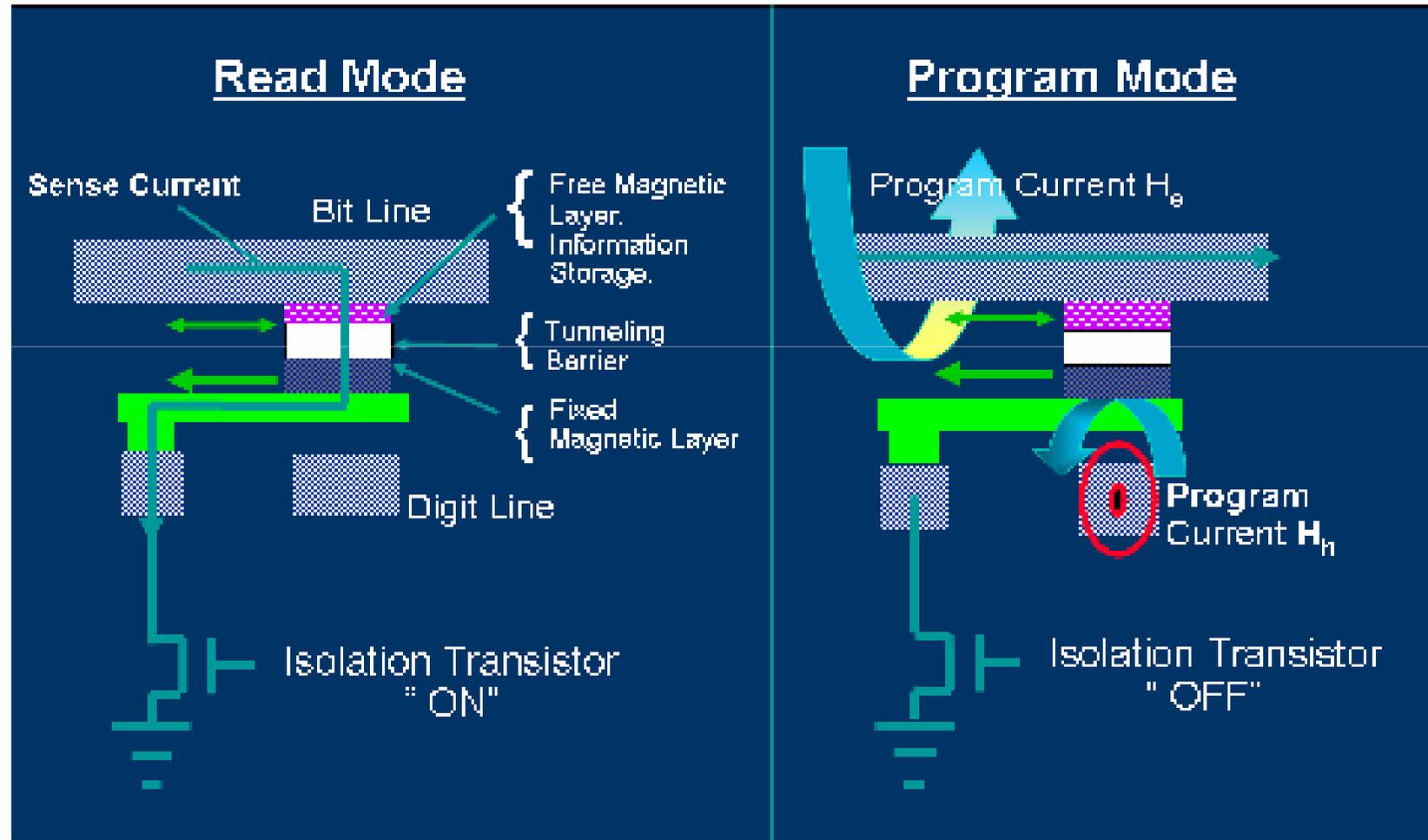
# Magnetic Tunnel Junction



Basic Structure of Exchange Biased MTJ



# MRAM: Major Application of MTJ



[Spintronics Class Lecture Notes, Stuart Wolf, Spring 2007]

# MRAM: Major Application of MTJ

## Potential Advantages:

- Compatibility with CMOS
- Density and speed of DRAM
- Less power than FLASH
- Unlimited writing cycles
- Truly Non-volatile

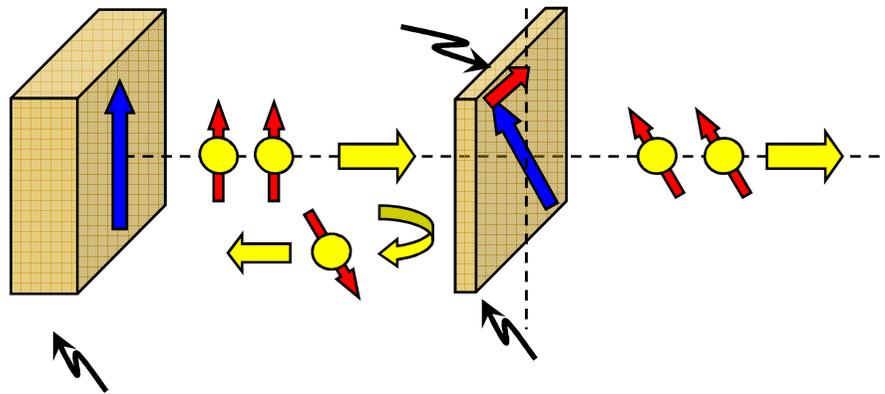
## Main Challenges:

Field Switching MRAM cannot be effectively scaled down (65nm node)!

- 1T-1MTJ cell structure limited by the size of transistor!

- Thermal Stability Factor:  $\frac{K_u V}{k_B T}$

# Spin Torque Transfer Switching



- A spin-polarized current injected into a ferromagnetic layer can induce a torque on its magnetization, hence rotate the magnetization.

**Key Advantage compared with conventional field switching:**

- Highly *Scalable* ← writing current scales down with cell size with constant  $J_c$ !

# Key Advantages and Potentials of STTRAM

	MRAM (180 nm)	DRAM (45 nm)+	SRAM (45 nm)+	FLASH (45 nm)+	STTRAM (45 nm)*
Cell size ( $\mu\text{m}^2$ )	1.25	0.03	0.18	0.03	0.03
Read time	35 ns	1 ns	0.5 ns	10 - 50 ns	5 ns
Write time	5 ns	1 ns	0.5 ns	0.1-100 ms	5 ns
Write energy/bit	150 pJ	0.02 pJ Needs refresh	5 pJ	10 nJ	0.04 pJ
Endurance	$> 10^{15}$	$> 10^{15}$	$> 10^{15}$	$> 10^{15}$ read, $> 10^6$ write	$> 10^{15}$
Non-volatile	Yes	NO	NO	YES	YES

- Excellent write selectivity ~ localized spin-injection within cell
- Highly Scalable ~ write current scales down with cell size
- Low power ~ low write current
- Simpler Architecture ~ no write lines, no bypass line and no cladding
- High Speed ~ Few nanoseconds

# Spin Torque Transfer Switching

Model by Slonczewski: 
$$J_c = \frac{2eM_s \delta \alpha (H + 2\pi M_s)}{h\eta}$$

$J_c \sim 10^8 \text{ A/cm}^2$  (Co:  $\delta = 2.5 \text{ nm}$ ,  $M_s = 1420 \text{ kA/m}$ ,  $\alpha = 0.1$ )

=> Too high to be practical! (  $10^6 \text{ A/cm}^2$  )

What we could engineer:

- $M_s$  Saturation Magnetization → Decrease
- $\alpha$  Gilbert damping parameter → Decrease
- $\eta$  Spin Transfer Efficiency → Increase

# Novel Barrier Exploration

- Only ~70% with  $\text{AlO}_x$ -MTJs.
- TMR record with MgO barrier: Over 300%!  
→ MgO increases  $\eta$  (spin transfer efficiency) significantly!

New Barriers Exploration → Increase  $\eta$  :

- Oxides:  $\text{VO}_x$ ,  $\text{TiO}_x$ ,  $\text{TaO}_x$
- Nitrides: BN
  - prevent the oxidation of under layer FM
  - large gap provides robust tunneling

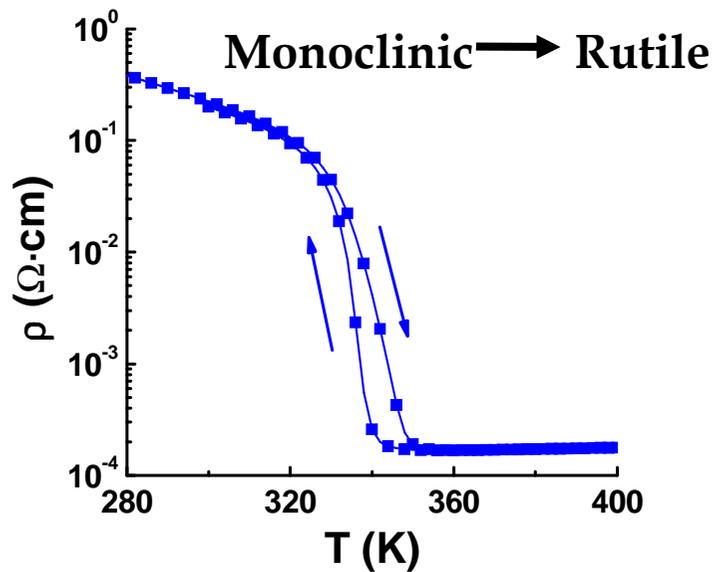
# Smart Barrier for MTJs

Challenge for SMT-MTJs:  
High  $J_c \rightarrow$  "Writing" voltage  
very close to junction break  
down voltage

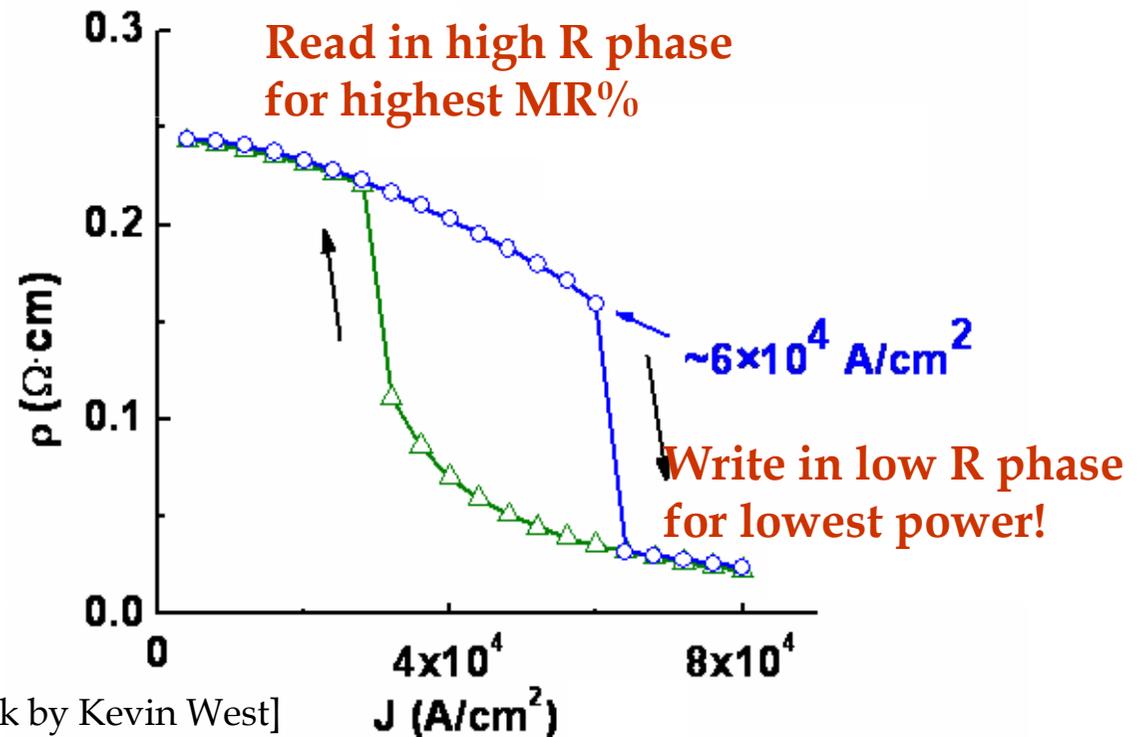


VO<sub>2</sub>:  

- Structural phase transformation from *Monoclinic* to *Rutile* at  $\sim 340\text{K}$
- Current Driven transition



Transition temperature:  $\sim 340\text{ K}$

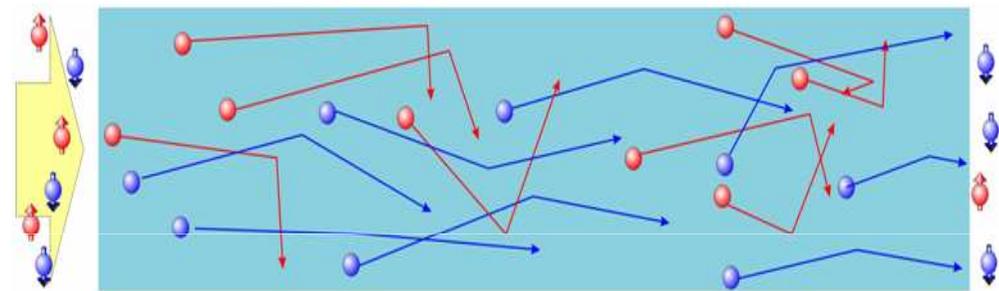
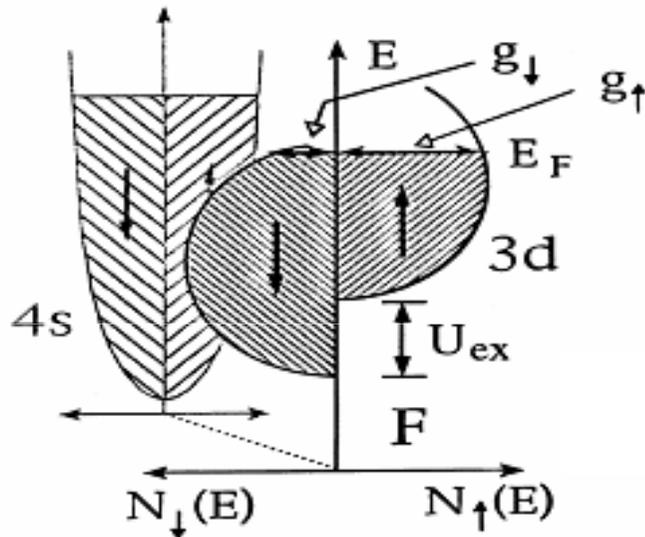


[Work by Kevin West]

# Outline

- Introduction and Motivation
- Background Theory
  - Spin-dependent Transport
  - Spin Polarized Electron Tunneling: FM-I-FM
  - AFM/FM Exchange Bias
- Experiment Setups
- Results & Discussion
- Summary & Future Plan

# Spin-dependent Transport

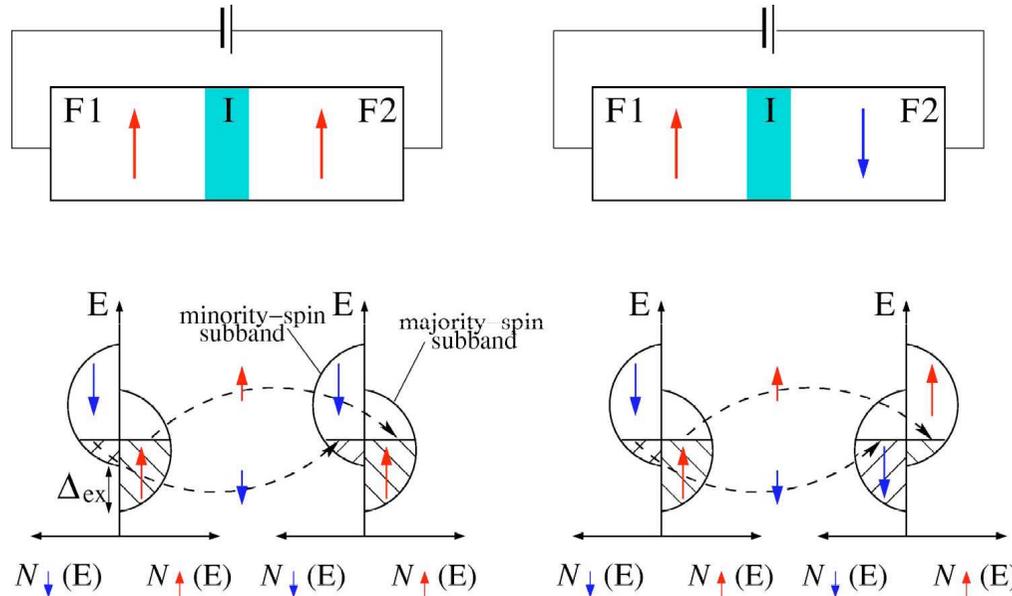


current through ferromagnetic metal

Density of State diagram for ferromagnetic metal:  $g_{\uparrow} > g_{\downarrow}$

[Spintronics Class Lecture Notes, Stuart Wolf, Spring 2007]  
 [Mark Jonson, *J. Phys. Chem. B* (2005), 109, 14278-14291]

# Spin Polarized Electron Tunneling: FM-I-FM



## Julliere's model:

- spin conserved tunneling
- $G_p = N_{1\uparrow}N_{2\uparrow} + N_{1\downarrow}N_{2\downarrow}$

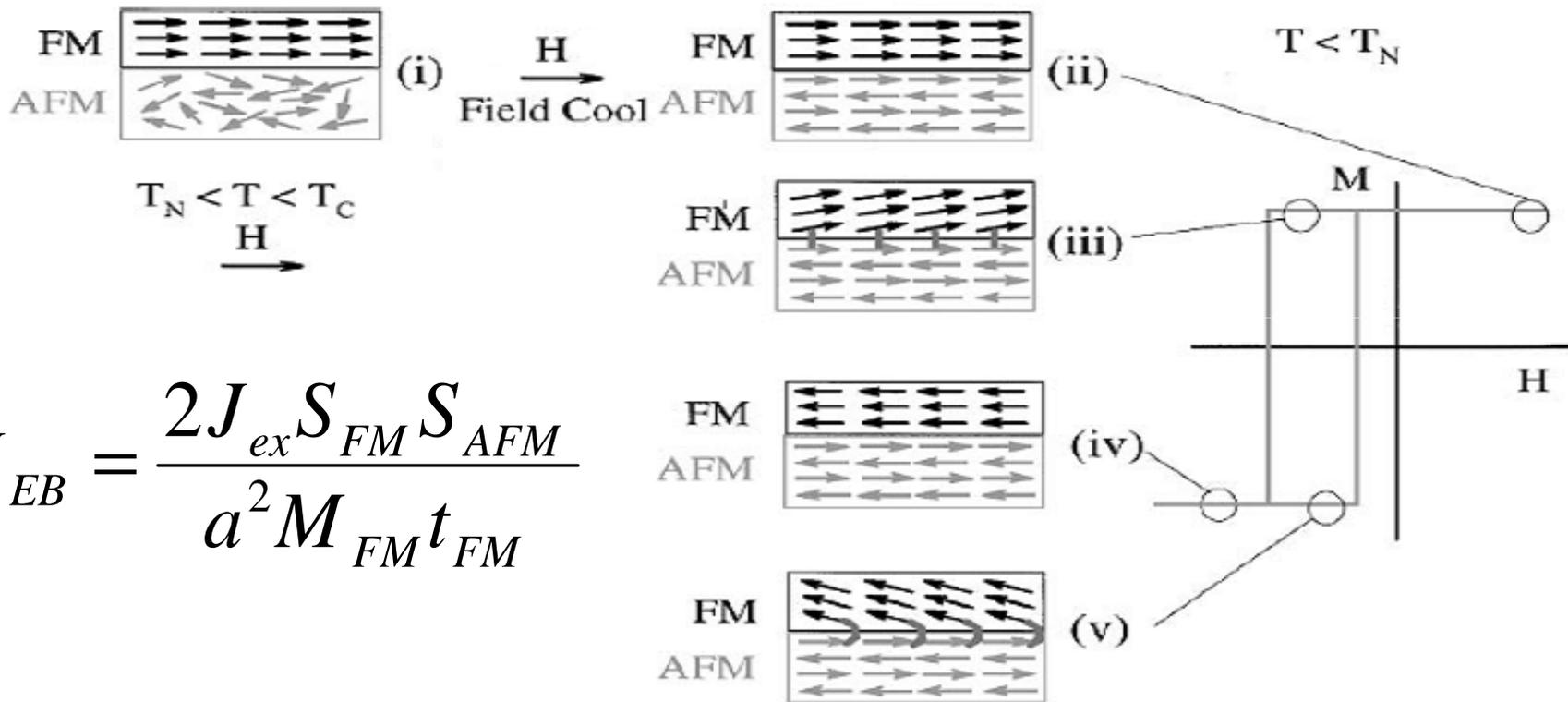
$$G_{AP} = N_{1\uparrow}N_{2\downarrow} + N_{1\downarrow}N_{2\uparrow}$$

$$P_1 = \frac{N_{1\uparrow} - N_{1\downarrow}}{N_{1\uparrow} + N_{1\downarrow}}$$

$$P_2 = \frac{N_{2\uparrow} - N_{2\downarrow}}{N_{2\uparrow} + N_{2\downarrow}}$$

$$TMR = \frac{\Delta R}{R_p} = \frac{R_{AP} - R_p}{R_p} = \frac{G_p - G_{AP}}{G_{AP}} = \frac{2P_1P_2}{1 - P_1P_2}$$

# Exchange Bias



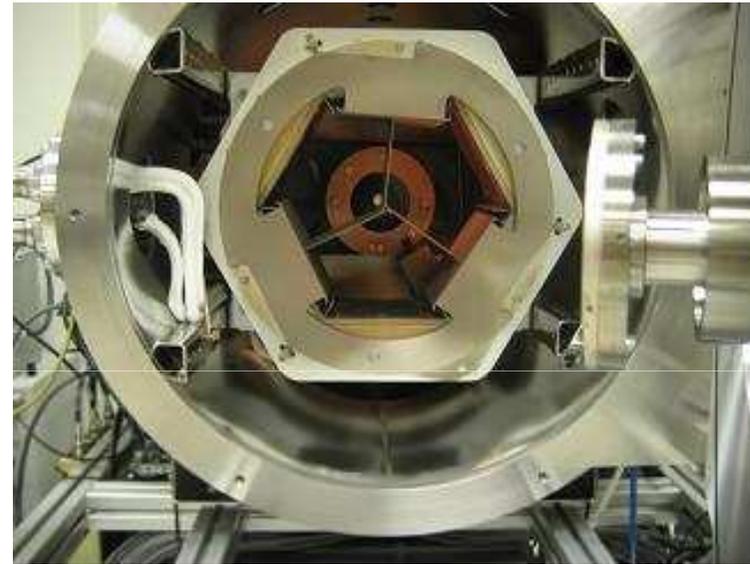
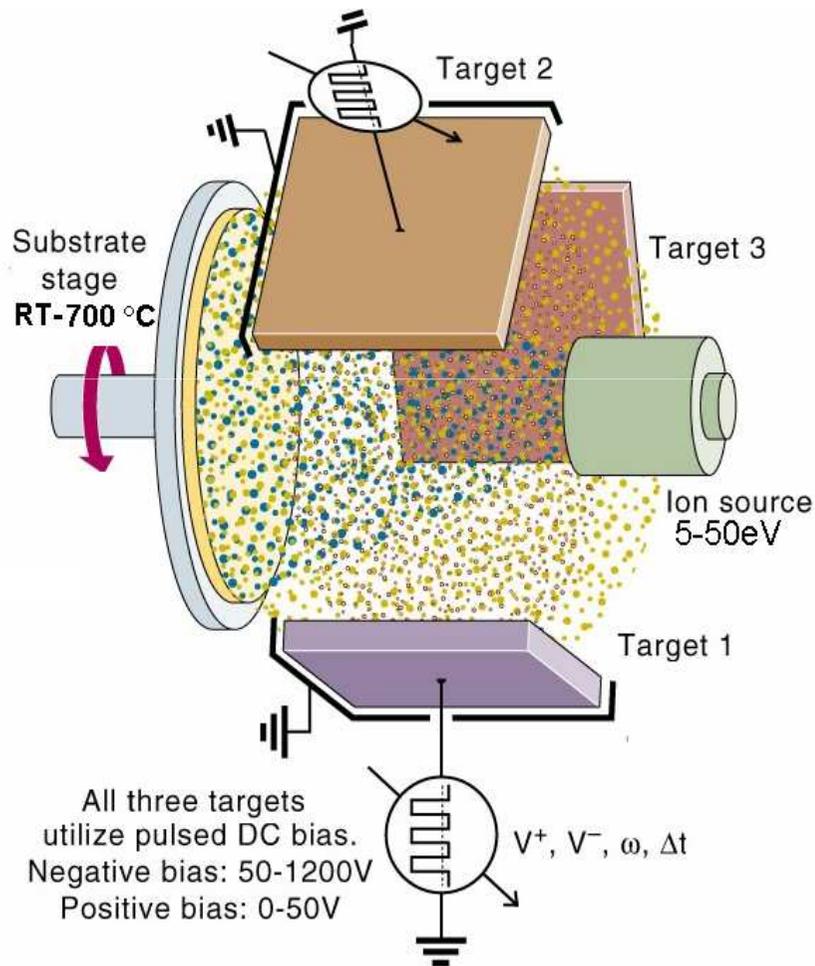
$$H_{EB} = \frac{2J_{ex} S_{FM} S_{AFM}}{a^2 M_{FM} t_{FM}}$$

[J.Nogues, Ivan Schuller, JMMM192(1999) 203-232]

# Outline

- Introduction and Motivation
- Background Theory
- **Experiment Setups**
  - Reactive Biased Target Ion Beam Deposition
  - Lithographic patterning process
  - CIPTech Measurement
- Results & Discussion
- Summary & Future Plan

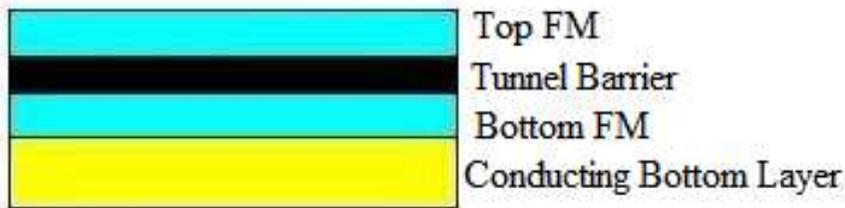
# Reactive Biased Target Ion Beam Deposition



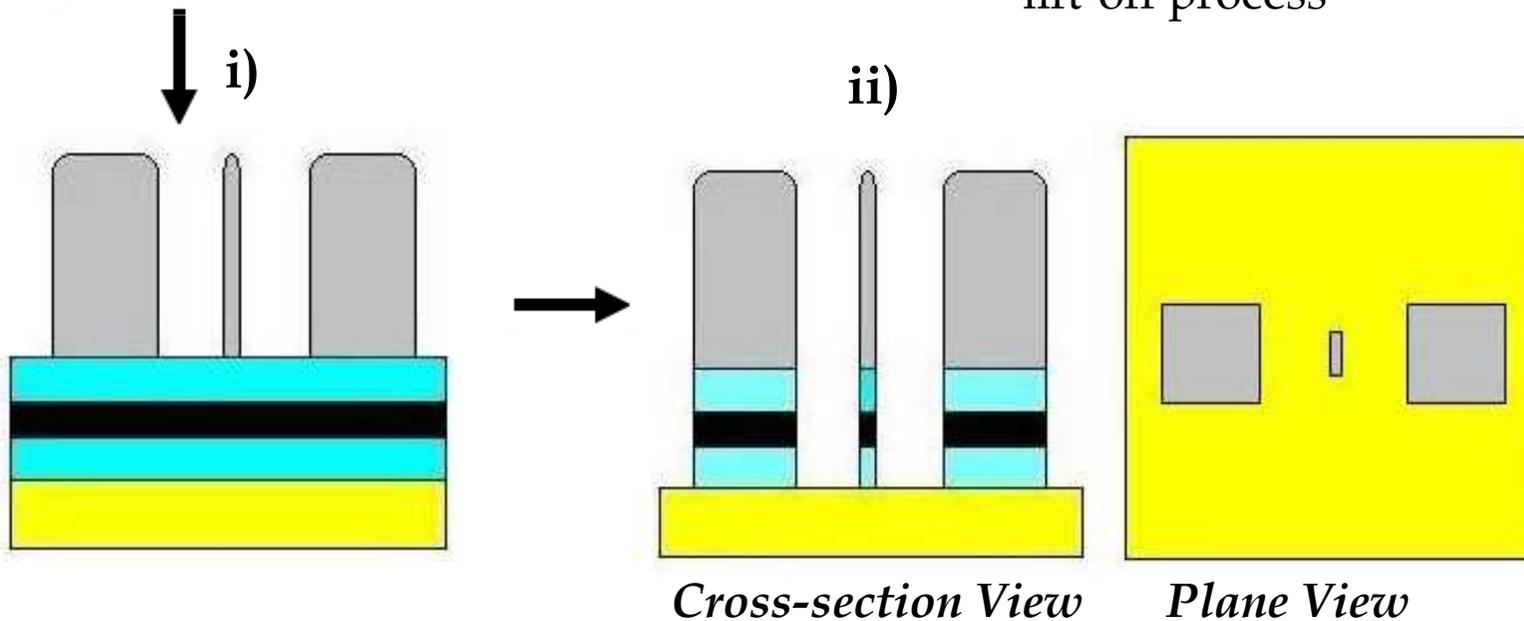
- Low Energy Ion Source (5-50eV)
- High Temperature  $\sim 700$  °C
- Smooth Surface/Interface Layer
- Control Phase Formation
- Combinatorial Growth  $\rightarrow$  Complex Oxides

# Lithographic Patterning (I)

## Unpatterned MTJ Film (*Cross-section View*)

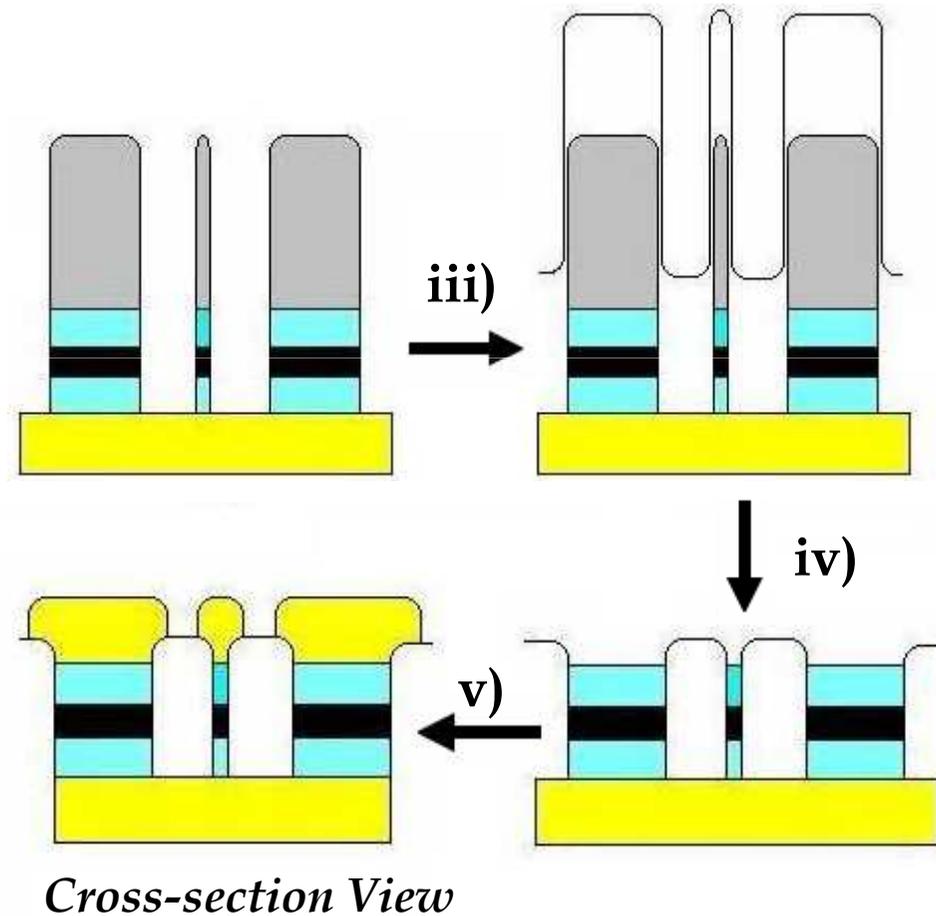
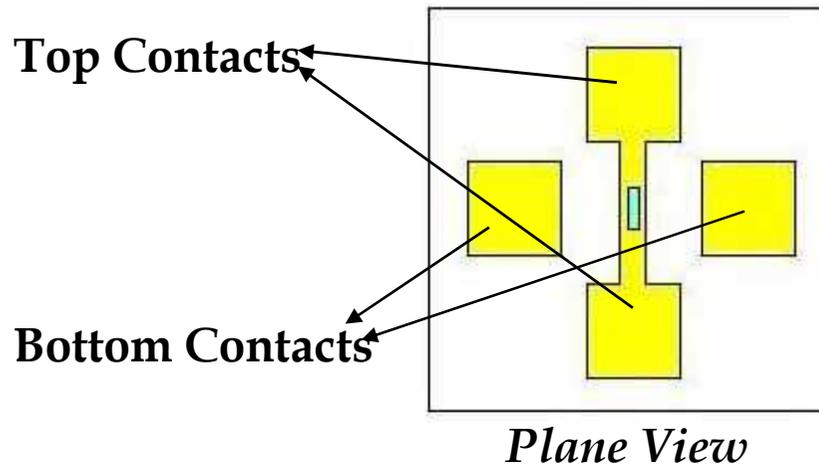


- i) Apply mask, develop photo resister (PR)
- ii) Dry etching to define junction structure; leave PR for next-step lift-off process

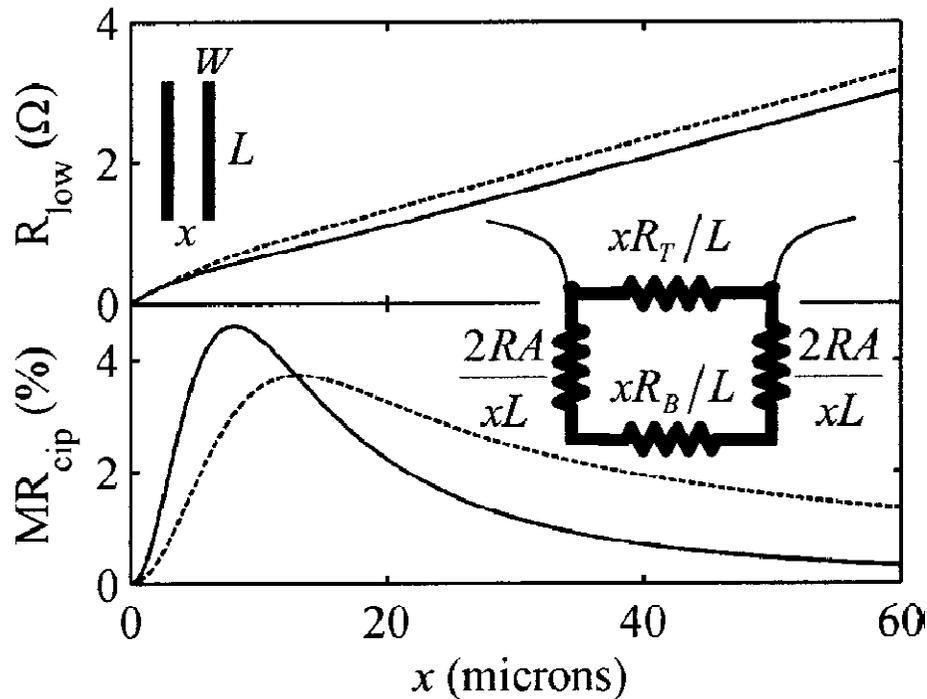


# Lithographic Patterning (II)

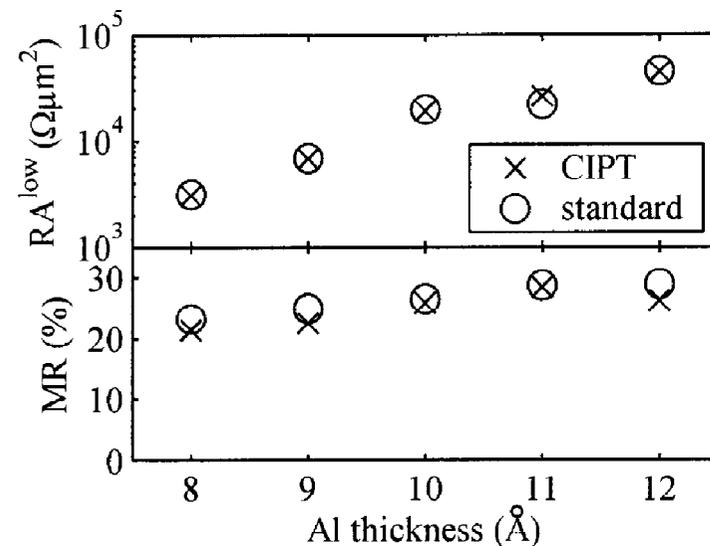
- **iii)** Deposition of  $\sim 300\text{nm}$   $\text{SiO}_2$  by rf-sputtering as passivation layer
- **iv)** Dissolve PR in Acetone to finish lift-off process
- **v)** Apply and develop another layer of mask, deposit and define Ti/Au contact layer by lift-off



# CIPTech Measurement



- *Fast, nondestructive, and accurate way to measure TMR without patterning!*
- Collaboration with NIST

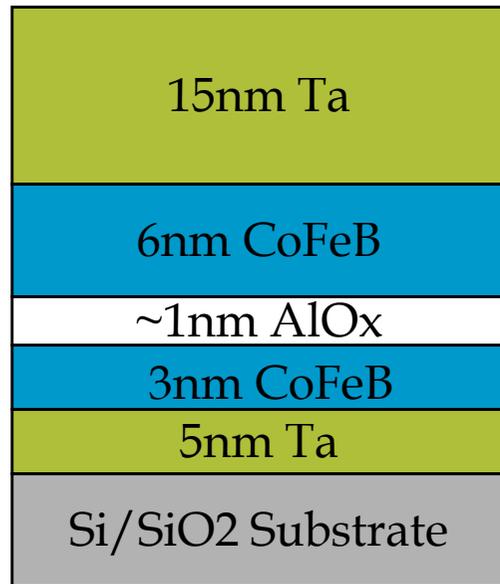


D. C. Worledge, etc. APL, **83**, 84 (2003)

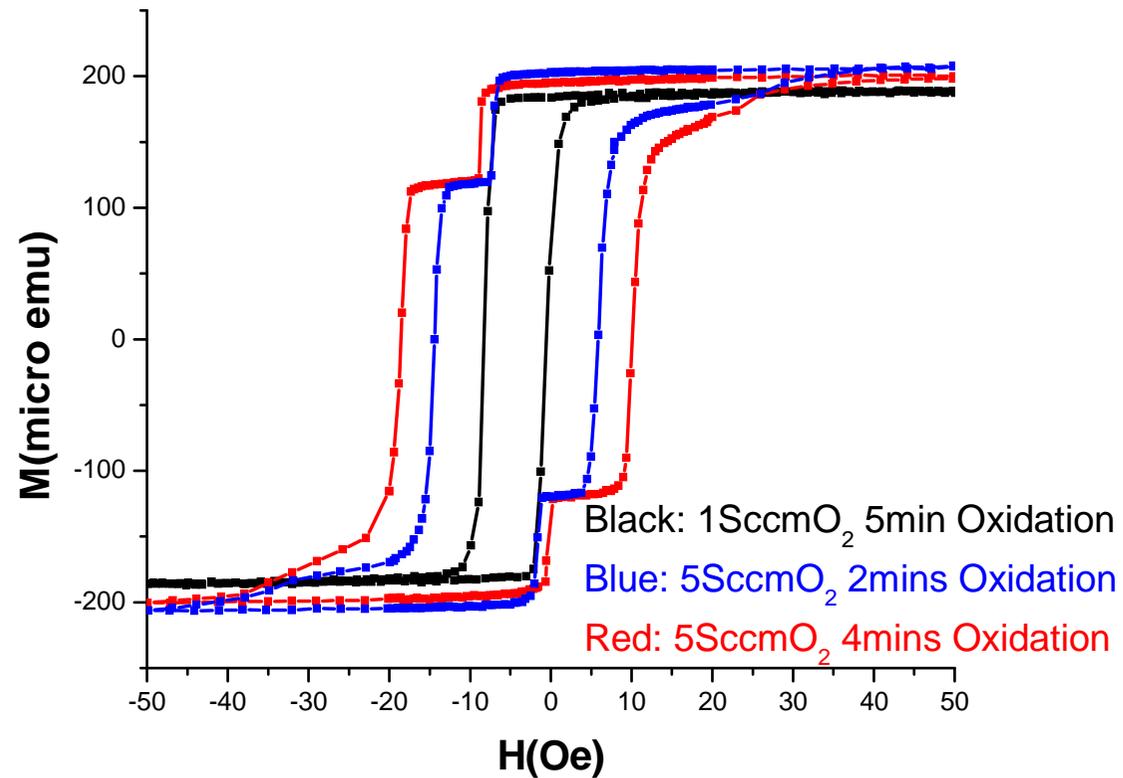
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# MTJ with AlO<sub>x</sub> Barrier (I)

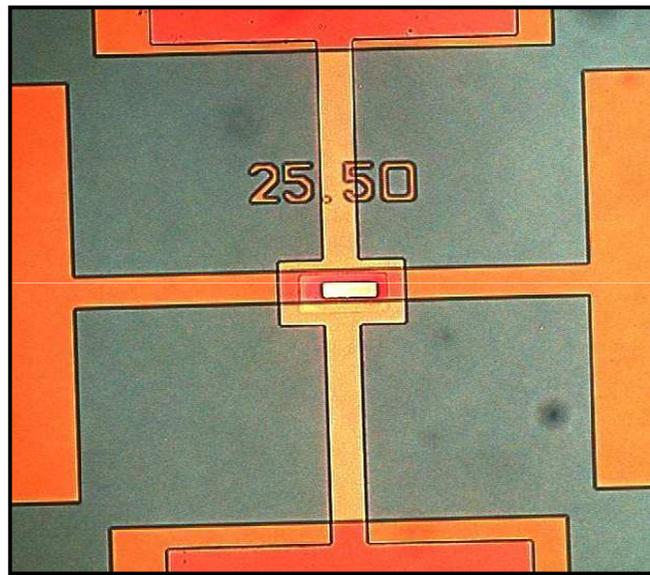


AlO<sub>x</sub>-MTJ Stack

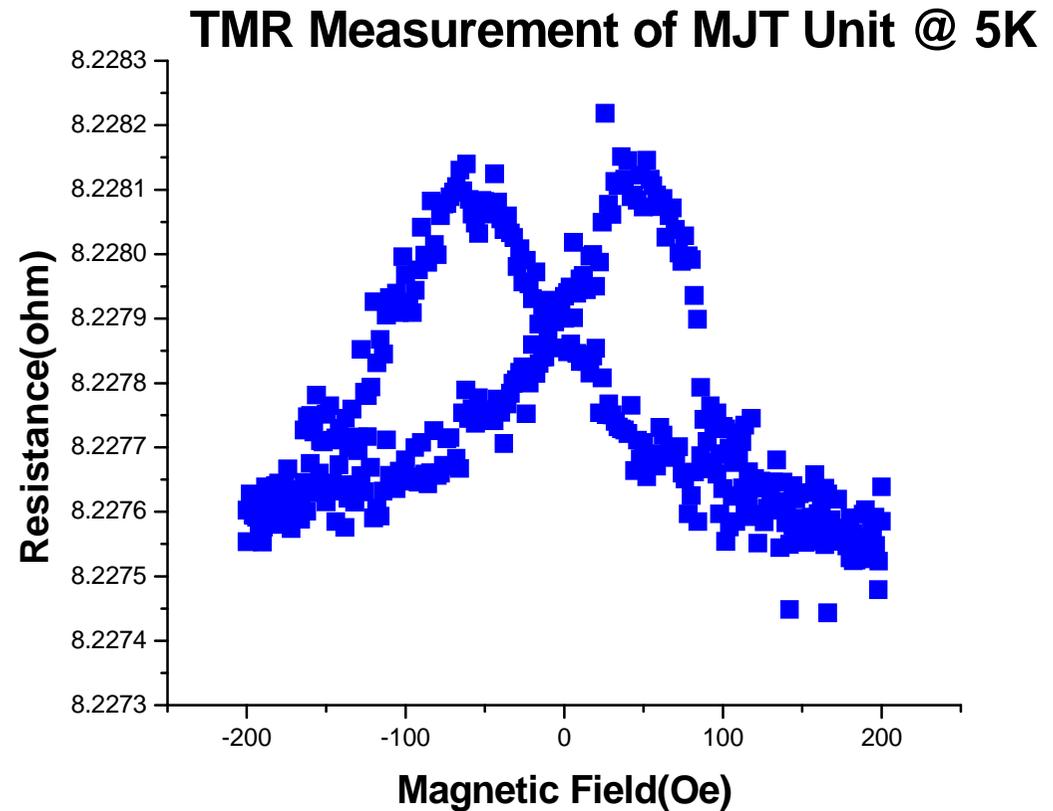


**Better oxidized AlO<sub>x</sub> barrier provides better separated switching!**

# MTJ with AlO<sub>x</sub> Barrier (II)



Microscopic image of patterned MTJ cell (25x50  $\mu\text{m}$ )

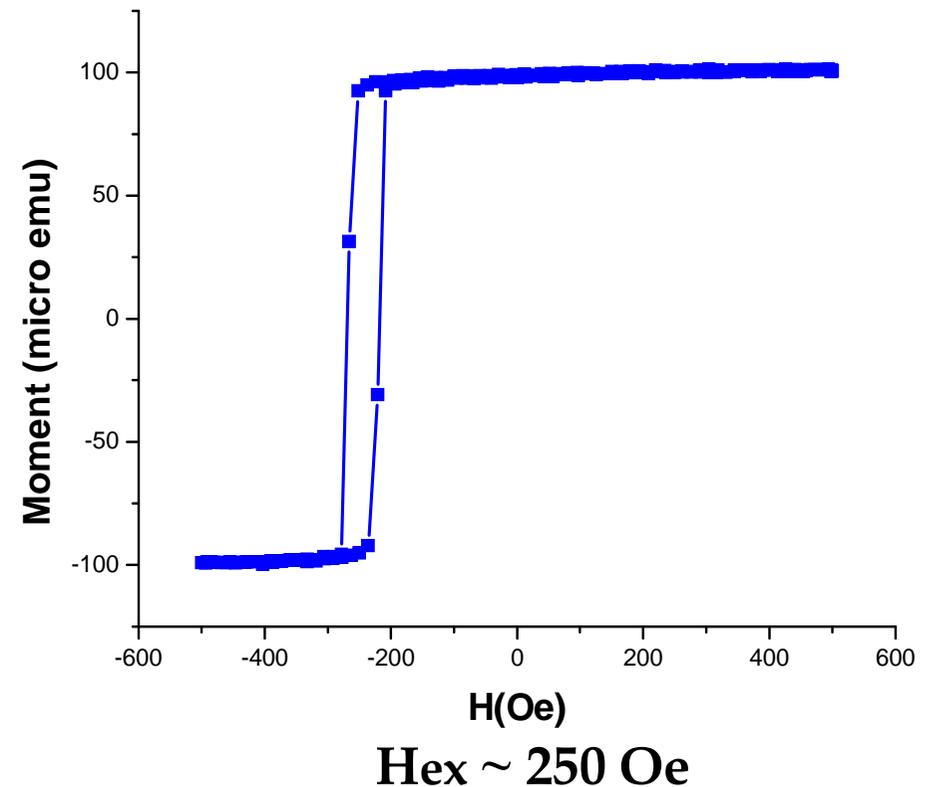
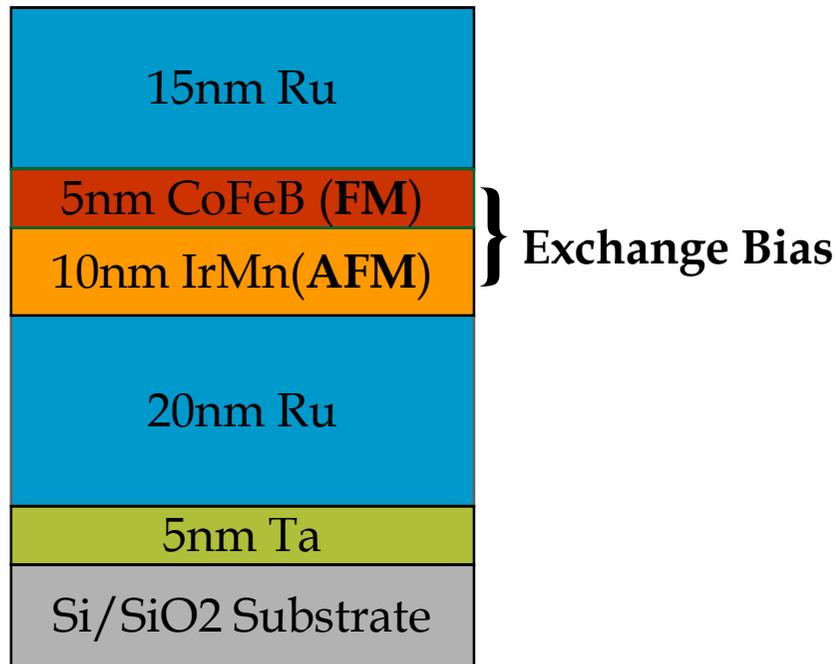


# VOx Recipe Development

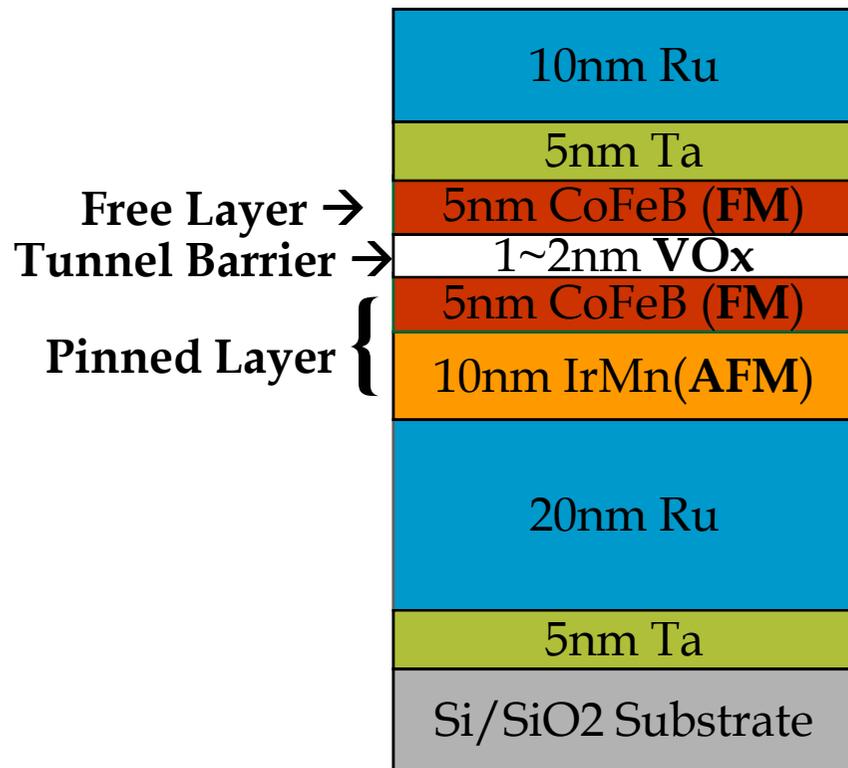
- Growth condition: on top of sub/CoFeB(1nm)/V(0.5nm)
- VOx thickness: ~50nm

Ar/O2 Flow Rate (Sccm)	Resistance (Ohm) Change (RT->~100C)
5.5	200K->30K
6	680K->150K
6.5	2,500K->400K
7	Too insulating
6 (with enhanced ion energy~50eV)	57K Ohm->200 Ohm (Temperature:50K->250K )

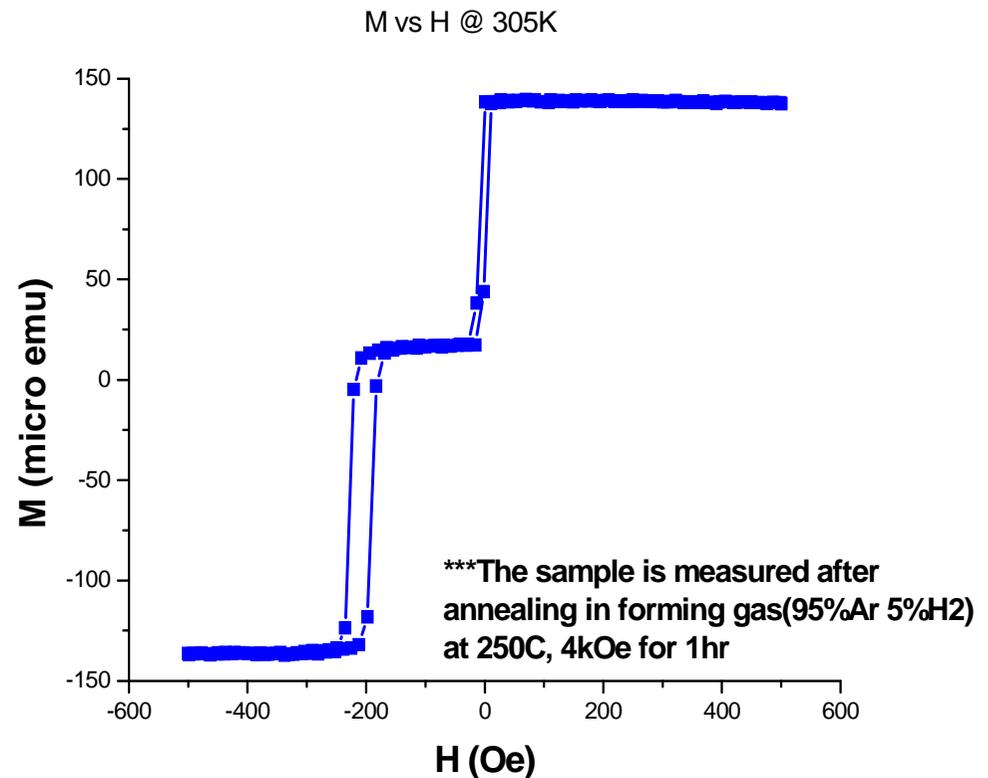
# IrMn/CoFeB Exchange Bias



# MTJ with VOx Barrier (I)



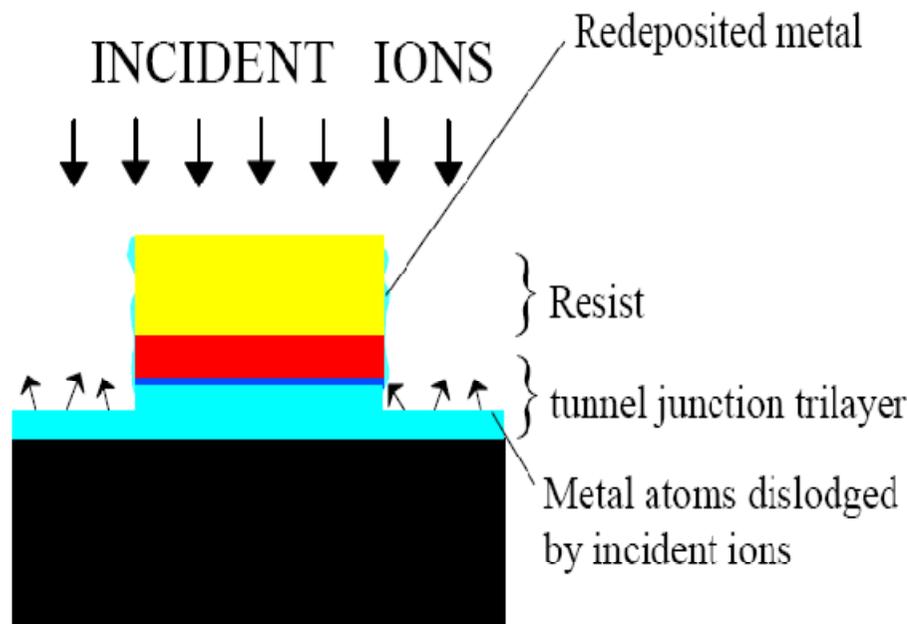
VOx-MTJ Stack



# Results Analysis and Improvement (I)

- Tunneling *interfaces* are crucial!
  - Over-oxidation of bottom FM layer
  - Alloy formation between FM and barrier material: pre-oxidation to form diffusion barrier
- *Barrier* needs to be further optimized!
  - Barrier Thickness: 1~2nm; Pinholes, uniformity problem with thin barrier
  - Oxidation approaches: natural oxidation, reactive sputtering, post-deposition plasma oxidation, etc.
- *Annealing* is also very important!

# Results Analysis and Improvement (II)



**Dry etching** is crucial in defining MTJ unit, and it could be further optimization!

→ **Solutions:**

- Using tilted rotating stage
- Reactive Etching Ar+Cl<sub>2</sub>

Utilizing more tools to facilitate the lithographic processing:  
**AFM, SEM, EBL, etc.**

# Summary

- Growth of Prototype  $\text{AlO}_x$ -MTJ
- Development of Basic Patterning Process
- $\text{VO}_x$  Material Exploration
- Preliminary  $\text{VO}_x$ -MTJ Experiments

# Future Work

- Continuous exploration of  $\text{VO}_x$ -MTJ; focusing on barrier growth and interface quality.
- Re-visit of  $\text{AlO}_x$ -MTJs to better understand the dependence of interface and barrier quality on TMR
- New barrier materials exploration: Oxides like  $\text{TiO}_x$ ,  $\text{TaO}_x$ , Nitrides like BN, etc.
- Further optimization of lithographic patterning process.